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710/260T (2182)
~~709/260T~~ (2152)

CLAIMS

1. A contactless IC card that sends/receives data to/from the outside and is supplied with power from the outside in a contactless manner, comprising:

a transmission circuit for sending/receiving data to/from the outside;

a buffer memory;

a DMA circuit for transmitting data received by said transmission circuit to said buffer memory and transmitting data stored in said buffer memory to said transmission circuit;

a nonvolatile memory;

a CPU for executing write/read processing on said buffer memory and said nonvolatile memory; and

state control means for halting operations of said nonvolatile memory and said CPU while said transmission circuit is sending/receiving data to/from the outside.

2. The IC card of Claim 1,

wherein a data bit appears every predetermined period in data sent/received by said transmission circuit,

said transmission circuit generates an interruption signal at timing between a period for sending/receiving one data bit and a period for sending/receiving another data bit, and

said DMA circuit executes transmission processing in

340/825 selective transponder
455 } transmission
370 }

response to the interruption signal.

3. The IC card of Claim 1,

wherein a data received by said transmission circuit has a structure in accordance with the standard of ISO/IEC 14443-3, and

said transmission circuit includes:

normal waveform storing means for storing a waveform pattern standardized by ISO/IEC 14443-3;

possible error waveform storing means for storing a waveform pattern including a possible error predicted with respect to a data received by said transmission circuit;

waveform detecting means for detecting a waveform pattern of a data received by said transmission circuit; and

collating means for correcting the data received by said transmission circuit on the basis of said normal waveform pattern when said waveform pattern detected by said waveform detecting means accords with said waveform pattern stored in said normal waveform storing means or said waveform pattern stored in said possible error waveform storing means.

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4. The IC card of Claim 1,

wherein a data received by said transmission circuit has a structure in accordance with the standard of ISO/IEC 14443-3,

said transmission circuit includes an analog circuit part for modulating a data received from the outside into a

digital data and outputting said digital data,

said IC card further comprises preset signal generation means for giving said analog circuit part a preset signal that is active during a period other than a period when said transmission circuit is receiving a data, and

said analog circuit part sets an output thereof to a logical high level in response to the active preset signal.

~~5. The IC card of Claim 5,~~

wherein a data received by said transmission circuit has a structure in accordance with the standard of ISO/IEC 14443-3,

said transmission circuit includes an analog circuit part for modulating a data received from the outside into a digital data and outputting said digital data,

said IC card further comprises hold signal generation means for giving said analog circuit part a hold signal that is active during a period other than a period when said transmission circuit is receiving a data, and

said analog circuit part sets, in response to the active hold signal, an output thereof to a logical high level during a period other than the period when said transmission circuit is receiving a data.

6. The IC card of Claim 1, further comprising a resume circuit for storing, when data write processing on said nonvolatile memory executed by said CPU is interrupted, a

proceeding state of the write processing up to time of interruption,

wherein said CPU resumes the write processing on said nonvolatile memory on the basis of said proceeding state stored in said resume circuit.

7. The IC card of Claim 1,

wherein said state control circuit includes a time counting circuit for starting counting time in response to said CPU going into a halt state, stopping counting the time in response to restoration of said CPU to an operative state and outputting a counted value to said CPU.

8. The IC card of Claim 1, further comprising a time monitoring circuit for starting counting time in response to said CPU going into a halt state and outputting a timeout signal to said CPU when said CPU does not restore to an operative state before a counted value reaches a given value,

wherein said CPU goes into the operative state in response to the timeout signal output by said time monitoring circuit.